

10.1 A mm-Wave CMOS Heterodyne Receiver with On-Chip LO and Divider

Behzad Razavi

University of California, Los Angeles, CA

The unlicensed band around 60GHz has motivated work on mm-wave CMOS building blocks such as low-noise amplifiers (LNAs) and mixers [1, 2] and oscillators [3]. However, the integration of these building blocks to form transceivers poses additional constraints on the design of these circuits. For example, a direct-conversion receiver would require at least two inductors for the LNA, one inductor for each quadrature mixer, at least two inductors for the quadrature oscillator, and at least one inductor for the first divider in the synthesizer loop. (In practice, each side of the quadrature oscillator must be loaded by a divider to retain phase balance, thus requiring one more inductor.) With the large foot print of the inductors, the 60GHz quadrature phases of the LO must travel a long distance before reaching the mixers (or, if the mixer transistors are placed next to the LO transistors, the RF signal must travel a long distance to reach the mixers.) Under these conditions, both the loss and mismatches contributed by the long interconnects degrade the performance of the LO and the receiver considerably. Insertion of buffers between the LO and the mixers does not resolve the mismatch issues as the buffers themselves must incorporate inductors. (The buffers are still necessary to avoid injection pulling of the LO by large in-band interferers received and amplified by the LNA.)

This paper describes a heterodyne receiver that avoids quadrature separation at mm-wave frequencies, easing the management of interconnect lengths and allowing the integration of all high-frequency building blocks.

Figure 10.1.1 shows the receiver architecture, where the RF mixer is directly driven by the LO and the IF mixers by half of the LO frequency. While designed for operation at 60GHz (with $f_{LO}=40\text{GHz}$), the fabricated prototype yields $f_{LO}\approx 35\text{GHz}$ and is tested with an input frequency of 53GHz. (A prototype with adjusted inductor values to allow operation at 60GHz is presently in fabrication.)

Several aspects of the above architecture merit consideration. First, in contrast to a 60GHz quadrature LO required in direct conversion, the oscillator used here must operate at 40GHz and provide only differential outputs. Therefore, it potentially achieves a lower phase noise especially because the Q of varactors appears to fall below that of inductors at high frequencies. Second, the choice of divide-by-2 [4] over divide-by-4 is governed by the level of image rejection that can be achieved by the selectivity of the front-end. Third, even though directly tied to the RF mixer, the LO is not pulled by in-band interferers because they bear a frequency difference as high as $f_{RF}/3$ with respect to f_{LO} . Fourth, the divide-by-2 circuit must operate at a nominal frequency of 40GHz, dictating either an injection-locked topology which suffers from a narrow lock range and hence poses risks on the overall design, or a Miller regenerative topology which does not readily produce quadrature phases. In this work, a Miller divider is chosen and the quadrature operation is performed in the IF signal path. As explained below, I/Q separation in the current domain negligibly affects the noise figure (NF) and gain of the receiver.

Figure 10.1.2 shows the implementation of the front-end. A cascode LNA is followed by a transconductance stage and a single-balanced mixer. The capacitances introduced by M_1 and M_2 at node X severely limit the bandwidth and raise the contribution of M_2 to the output noise. Thus, in a manner similar to the mixer design in [1], an inductor is connected to node X to resonate with the total capacitance at this node. Current source I_X ($\approx 0.25I_{D1}$) provides some flexibility in the noise and gain optimization of the stage.

The magnetic coupling factors indicated between L_1 ($=180\text{pH}$) and L_2 ($=60\text{pH}$) and between L_3 ($=192\text{pH}$) and L_4 ($=287\text{pH}$) result from "nesting" these inductors. The return paths of the signal currents carried by L_3 , L_4 , and L_5 ($=192\text{pH}$) must be chosen carefully so that parasitic inductances do not degrade the Q or raise the value of these components. This is accomplished by means of metal sandwich capacitors C_1 and C_2 , which are tied to a wide ground plane that extends 100 μm and connects to the input ground pads.

In order to accommodate a nominal center frequency of 60GHz, the mixer may employ an inductor tied to the common-source node of the switching pair while carrying some of the bias current of the input transconductance device [1]. However, in the presence of mismatches between current sources, it becomes difficult to guarantee a well-defined current through the switching pair. To resolve this issue, the front-end of Fig. 10.1.2 capacitively couples the signal current of M_3 to the mixer core while L_5 resonates with the capacitances at nodes A and B [5]. Thus, the noise and nonlinearity performance of M_3 is decoupled from the switching efficiency of M_4 and M_5 . The load inductors L_6 and L_7 (realized as one symmetric structure) provide both conversion gain and suppression of LO (which would otherwise desensitize the IF mixers.)

Figure 10.1.3 depicts the IF mixers. As with the RF mixer, this circuit isolates the bias of the switching transistors from that of the input transconductance stage. The IF current generated by this stage is applied to a current-mode quadrature-phase-separation network R_1 - R_2 and C_1 - C_2 , with the resulting outputs commutated by the switching quads. Since the finite impedance seen at the common source nodes of the switching quads introduces a small error in the phase separation, capacitors C_3 and C_4 are added to provide partial correction.

While splitting the IF current between the two switching quads, the phase-shift network does not degrade the overall gain or NF significantly. This can be seen by viewing M_1 or M_2 in Fig. 10.1.3 as equivalent to two transistors in parallel, which would be required in typical quadrature down-conversion mixers driven by quadrature LO phases. In other words, it is as if the input transconductance stages of two mixers are merged into one.

The receiver is fabricated in a 90nm digital CMOS technology and tested on a high-frequency probe station. Figure 10.1.7 shows the die, whose active area is approximately $400\times 300\mu\text{m}^2$. Figure 10.1.4 plots the measured NF, voltage gain, and I/Q imbalance as a function of the input frequency, and Fig. 10.1.5 shows the measured baseband waveforms, indicating a phase mismatch of 5.5° and a gain mismatch of 1.5dB. Fig. 10.1.6 compares the measured performance of the prototype with that of the 60GHz receiver reported in [6].

Acknowledgements:

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References:

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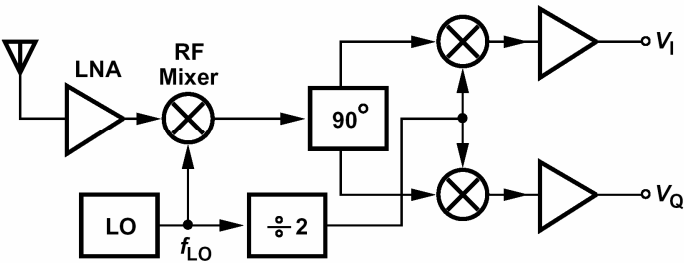


Figure 10.1.1: Receiver architecture.

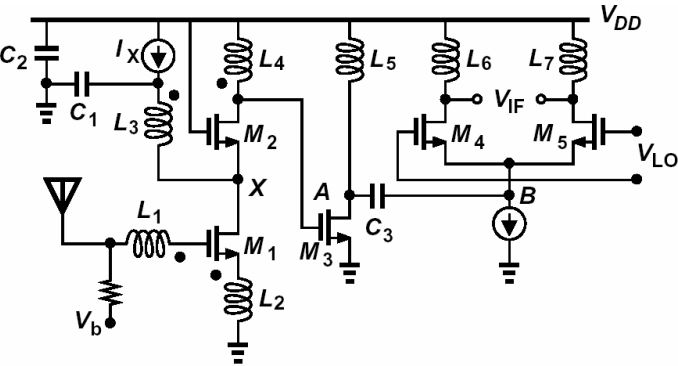


Figure 10.1.2: Front end design.

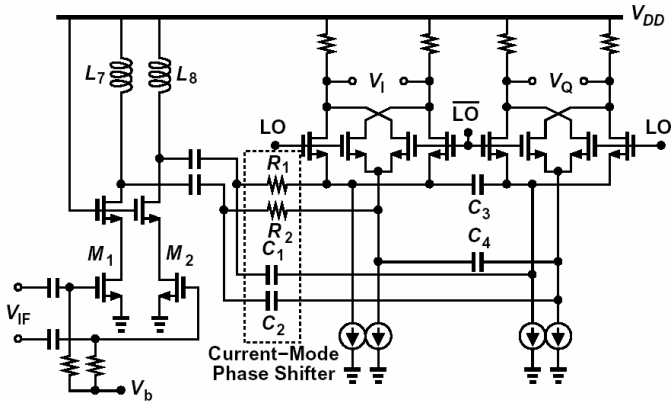


Figure 10.1.3: IF mixers.

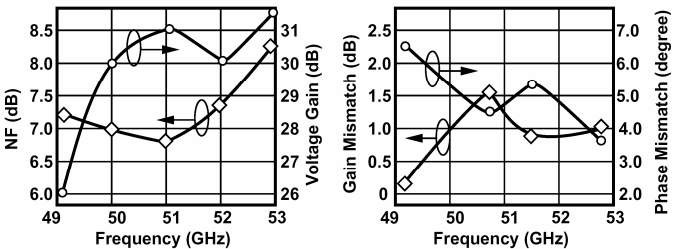


Figure 10.1.4: Measured NF, gain, and I/Q imbalance.

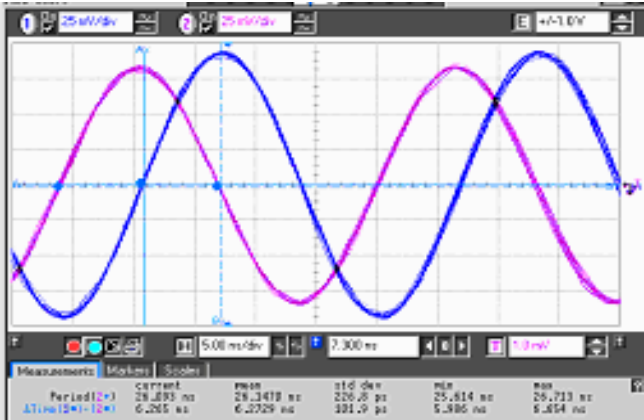


Figure 10.1.5: Measured quadrature outputs in baseband.

	Receiver in [6]	This Work
Noise Figure	5–6.7 dB	6.9–8.3 dB
Voltage Gain	38–40 dB	26–31.5 dB
1-dB Compression Point	–36 dBm	–25.5 dBm
LO Leakage to Input	NA	–47 dBm
Image Rejection ratio	30 dB	44.5 dB
I/Q Mismatch	1 dB/4°	1.6 dB/6.5°
LO Phase Noise @ 1-MHz Offset	–90 dBc/Hz	–95 dBc/Hz
Power Dissipation	450 mW *	80 mW
Supply Voltage	2.7 V	1.8 V
Technology	200-GHz BiCMOS	90-nm CMOS

* This value excludes the synthesizer power dissipation to allow a fair comparison between the two cases.

Figure 10.1.6: Comparison of performance.

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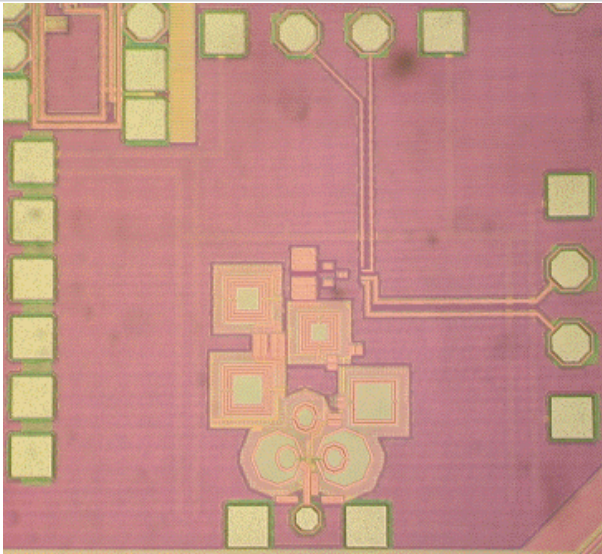


Figure 10.1.7 Die micrograph.